Experimental validation of current limitation methods for grid forming inverters

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***Abstract* — This paper discusses possibilities of current limiting mechanisms for grid forming inverters. One method is integrated into an existing inverter control system, where correction values are added to the virtual synchronous machine control in amplitude and, if necessary, in phase angle. The functionality of current limiting is afterwards demonstrated in laboratory tests. At first, tests are carried out considering a reduction of the voltage amplitude for fault modelling. In further tests, a test network with a grid fault event is then simulated using a power hardware-in-the-loop system. The concept for the current limitation in grid fault situations shows that it is possible to limit over-currents while maintaining the dynamic behaviour of grid forming inverters.**

Keywords — grid forming inverters, grid forming control, fault-ride-through, current limitation

I. Introduction

The consistently increasing share of renewable energy systems in total power generation is leading to a change of the dominating feed-in technology in the grids [1]. Whereas conventional power plants are characterized by synchronous generators, renewable energy sources are mainly connected to the grid through inverters. Since many aspects of grid ancillary services as well as physical properties that form the basis of system stability are based on the characteristics of a conventional synchronous machine, their gradual replacement will lead to new challenges in grid operation. In conventional power generation, electrical energy is mostly generated in large fossil fuel power plants by synchronous generators, so that their technology-related operating behaviour determines the control and operational management to maintain grid stability. In comparison, renewable energies, especially photovoltaic and wind energy plants, are connected to the grid via inverter systems [2]. Since the operating behaviour of power electronic generation systems and rotating generators is different, the approach is to adapt inverters to the usual grid control or to emulate the dynamic behaviour of a synchronous generator. The inverters already used in the interconnected grid are designed in order to feed the generated power into the grid as efficiently as possible instead of contributing to grid stability [2]. These inverters are synchronized with the grid voltage and feed a certain amount of active and reactive current into the grid in order to supply their maximum power from renewable energy sources.

In order to use inverters that can emulate the behaviour of synchronous generators and contribute to the stability of the grid, there has been an increasing focus on grid forming inverters (GFI) in recent years. Due to the fundamental behaviour of a voltage source, an inherent reaction likewise a synchronous machine can be achieved [3]. The field of application is usually a stand-alone supply in island grids. In order to guarantee a safe coupling with the mains it is necessary to have a superior control emulating the elementary behaviour of synchronous generators. This control will provide inertia in order to reduce frequency deviations. Thus, instead of using conventional power plants to provide the services of inertia, grid forming inverters with virtual synchronous machines controls can be used to stabilize the grids through inertia services [1]. However, since the inverter has a technical maximum current due to its hardware, the current must be limited by means of a control in situations with typically large currents such as short circuits. While synchronous generators, due to their physical structure, can briefly feed excessive over-currents into the grid without damaging or destroying the unit, power electronic systems are generally not designed to operate above the rated current and a grid fault in a grid forming inverter would immediately lead to a significant increase in the output current with consequent equipment damage. Therefore, in order to maintain power supply continuity, grid faults have to be run through, so there is a need to limit the output currents in grid fault situations [2]. In order to be able to continue to maintain grid-stabilising behaviour, the grid forming characteristics need to be maintained.

The control of grid forming inverters in grid parallel operation is still in the research and development phase, so that no consistent requirements and specifications for technical implementation have yet been defined. Also, for the basic behaviour during current limiting, different approaches have been followed so far. While in this field many control concepts propose a change to the usual current-influencing mode or the implementation of an underlying current control, this paper will discuss a control model that corrects the voltage amplitude and preserves the grid-stabilising behaviour as much as possible.

II. Grid Forming Inverter controls in short circuit situations

In order to evaluate the dynamic behaviour, grid forming controls are presented. Then their behaviour during a grid failure is analysed.

A. Control of grid forming inverters

During the operation of a GFI in parallel mode to the grid, special attention needs to be paid towards keeping the GFI voltage synchronized with the grid in order to avoid high compensating currents. Therefore, a virtual synchronous machine control which emulates the behaviour of a synchronous machine, is required. An overview of different grid forming inverter controls can be found in [4]. One selected model is used for this purpose and is presented below, see for details [5] and [6]. This control consists mainly of two different parts: the frequency controller and the voltage controller. An overview of this model is depicted in Fig. 1.

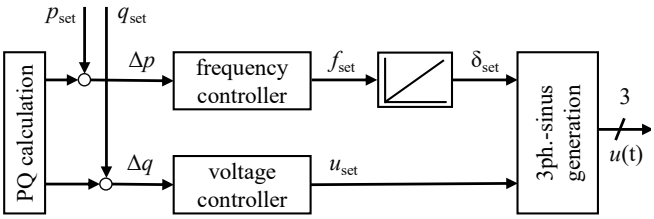

Fig. 1. Control structure of a grid forming inverter with virtual synchronous machine control

Using the PQ calculation, the output power is calculated as p.u. values. The active and reactive power in p.u. are then subtracted from the setpoints p_{set} and q_{set} in each case and the control difference is then transferred to the frequency and voltage controller. The difference in active power Δp is processed by the frequency controller into a new setpoint frequency f_{set}, which is then converted by an integrator into the space vector phase angle δ_{set}. On the other hand, a new set voltage amplitude is formed from the reactive power difference Δq via the voltage controller. The voltage amplitude and the space vector angle are then combined to create a three-phase symmetrical voltage for the PWM inverter.

B. *Transient behaviour in grid fault situations*

In addition to the control for undisturbed operation, GFIs must be able to operate during grid fault situations. If a GFI is operating within a rigid grid environment, the inverter is sensitive to rapid changes in the grid conditions, such as short circuits or generation and load disruptions. The procedure during the fault situations can be illustrated using a simplified equivalent network diagram of a grid situation. Fig. 2 shows an equivalent circuit diagram in which the GFI is represented by an AC voltage source u_{inv} with filter reactance X_{filter}.

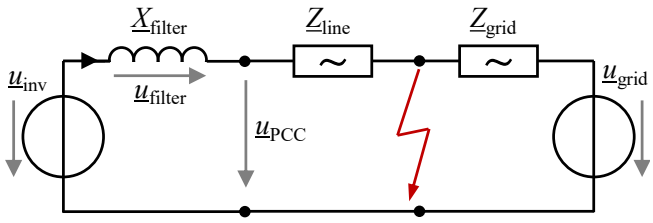

Fig. 2. Simplified model of a GFI in grid parallel operation during a short circuit event

The GFI is coupled via the grid impedances Z_{line} and Z_{grid} to another AC voltage source u_{Grid}, which represents the external grid. The short circuit occurs between the grid impedances, so that at the PCC of the GFI the output voltage u_{PCC} is not equal to zero. Fig. 3 shows the vector diagrams belonging to Fig. 2 for a short-circuit case without current limitation (a) and with current limitation (b).

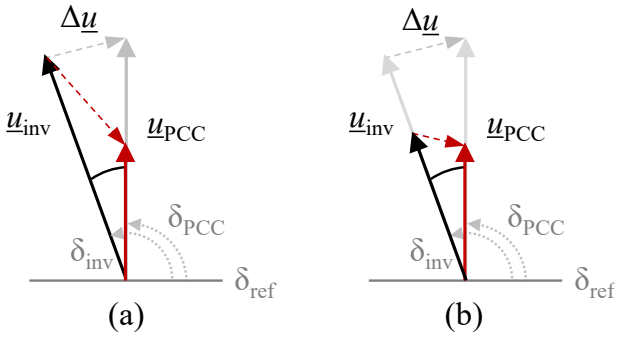

Fig. 3. Phasor diagrams of a GFI in grid parallel operation during a short circuit event (a) without and (b) with current limitation

The short-circuit causes a voltage drop from u_{PCC} in grey to the u_{PCC} red phasor by rapidly decreasing its amplitude. In case the GFI does not react with an adjustment of the amplitude as shown in Fig. 3 (a), a large Δu is caused by the phasor diagram, which carries a large current via the impedance. This leads to over-currents in the GFI, which can trigger the overcurrent protection and lead to the disconnection from the mains. Therefore, as shown in Fig. 3 (b), the amplitude must be adjusted in order to reduce Δu and therefore reducing the output current of the GFI via (1).

$$\underline{i}_{inv} = \Delta\underline{u} / (\underline{Z}_{filter} + \underline{Z}_{line} + \underline{Z}_{grid}) \quad (1)$$

Since the impedance Z is a fixed value, the voltage Δu has to be reduced so that the resulting current is sufficiently limited. Although the filter impedance Z_{filter}, which can also be described as $Z_{filter} = X_{filter}$, is known, Z_{line} and Z_{grid} have variable values. In this consideration it is assumed that a voltage drop due to a short circuit in the grid is merely represented through a reduction of the voltage amplitude. This analysis starts from the assumption that a voltage drop due to a short circuit in the grid can be represented by a single reduction of the voltage amplitude. An adjustment also for the phase angle is shortly described in the following chapter and is discussed in more detail in chapter V.

III. Current Limitation Methods for Grid Forming Inverters

As it has already been shown, due to the control as a voltage source, even small phase angle changes or voltage dips can lead to a significant change in the power exchange and thus to a significant increase in the output currents. This applies in particular to controls which keep the set voltage of the GFI u_{Inv} constant. Inverter systems are equipped with a hardware protection that disconnects the inverter from the grid in over-current situations to prevent thermal damage to the power electronics. However, especially in grid fault situations, these systems have to stay synchronised to the grid to ensure the continuity of power supply. For state-of-the-art inverters several studies have been made [7][8] and was also specified in grid codes in fault-ride-through (FRT) requirements [9].

A. *Literature review*

In addition to the hardware protection, there are other methods of limiting the output current using the controls of the inverter. In order to be able to adjust the behaviour in the event of a grid fault in more detail, software-based protective methods are available which provide a new voltage reference to the hardware-based control system. In [10] and [11], a method is presented which changes from the voltage-controlled inverter control to the current-controlled inverter control in the event of a fault. However, this eliminates the advantages of instantaneous reaction to changes in grid state. In addition, instantly switching between the modes is considered to be impossible and two operating modes have to be available on the GFI controller, which increases plant costs. [12]

In other concepts, the voltage controller of the GFI has an internal current control in addition to the voltage control loop. In [12], for example, the authors publish a concept based mainly on setting the integral part of the internal current regulator to zero for the faulty phase as soon as a fault situation is detected. Other concepts, e.g. in [13], are based on the principle of virtual impedance. This creates a virtual voltage drop across the virtual impedance, which reduces the voltage reference transmitted to the PWM so that the currents being fed are limited. In [14] on the other hand, the new voltage reference value is determined indirectly via the measured voltage at the PCC in the event of a short circuit by determining the new filter voltage required for the short circuit trigonometrically. However, this method is not suitable for overload situations, since the voltage at the terminals hardly changes in case of overload. The advantages of the latter two concept approaches are that the characteristic grid-stabilising behaviour is maintained as far as possible, no additional hardware has to be installed and the power dissipation does not increase.

B. *Implementation of the current limitation in the existing inverter control*

Moreover, a function for current limitation is integrated into the existing model from Fig. 1. The requirements were to minimise changes to the existing control and to be able to use it for other approaches for grid forming inverter controls. The corresponding block diagram is shown in Fig. 4.

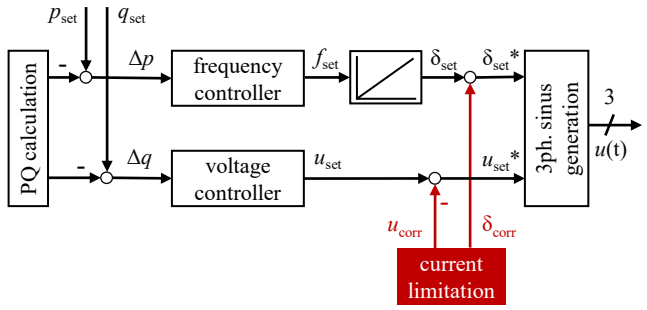

Fig. 4. Integration of current limiting function into the existing GFI model

Here, a block for current limitation is added to the scheme, which reduces the amplitude of the set voltage u_{set} by an additional correction value in order to limit the output currents. The voltage correction value u_{corr} is determined from the measured output current i_{inv} and the measured voltage u_{PCC}. This value is then subtracted from the voltage correction value u_{set}. Finally, the corrected voltage value u_{set}* is given to the setpoint generation block, in which the sinusoidal output voltage is generated. Already the reduction of the amplitude with unchanged phase position during the fault has already shown to be insufficient during first tests. Depending on the state variables (grid topology, load state, type of short circuit, etc.) which predominate before the occurrence of the short circuit, the oscillation of the angle between u_{Inv} and u_{PCC} may lead to instability. In order to sustain synchronism, it is also necessary to adjust the phase angle by a factor δ_{corr}. This angle is added to the phase δ_{set} generated by the frequency controller, so that finally δ_{set}* is passed on for sine wave generation.

The resulting behaviour is shown in the equivalent circuit diagram and the phasor diagram of the inverter structure in Fig. 5.

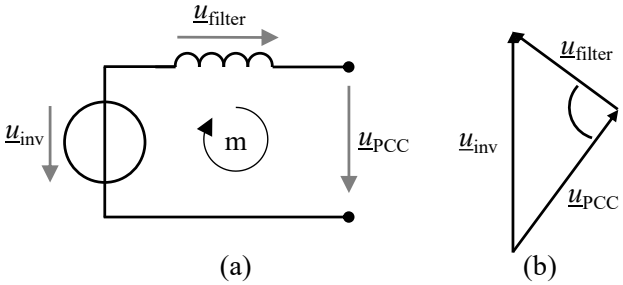

Fig. 5. (a) Equivalent circuit diagram and (b) phasor diagram of the dynamic behaviour of a GFI

Assuming that the filter of the inverter has an inductive behaviour, the setpoint voltage of the inverter $\underline{u}_{inv}$ is determined by the measured voltage at the connection point $\underline{u}_{PCC}$ reduced by the filter voltage $\underline{u}_{filter}$ using the mash equations from Fig. 5 (a). When focussing on active power supply, the new voltage setpoints can be approximately determined by the trigonometrical function according to Fig. 5 (b). A control scheme is depicted in Fig. 6.

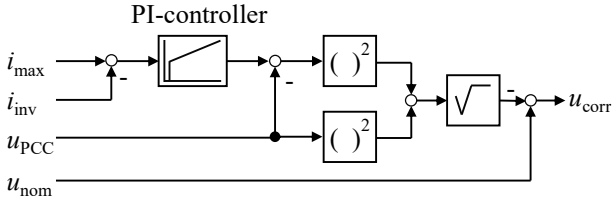

Fig. 6. Block diagram for the calculation of the correction value of the voltage amplitude using a trigonometric function

The difference between i_{max} and the measured i_{inv} is processed by a PI controller and subtracted from the measured voltage u_{PCC}. The square of the result is then added to the square of u_{PCC} and the square root is determined from it. From the actual voltage u_{nom} the result is subtracted again to get the voltage correction value u_{corr}.

Besides, it has turned out to override the voltage controller during a fault situation for a certain time. In the studies carried out, a duration of 80 ms was chosen. This is especially useful for restoring the voltage to normal after the fault clearance. As soon as the current limitation is active, u_{set} is only slightly reduced by the voltage controller due to the override, which means that the control difference between u_{set} and u_{PCC} for the process of the fault clearance is also small. This results in

reduced compensation currents at the moment of fault clearance. In addition, this ensures that the controllers have no negative interaction with each other. Although the time constants of the controllers have different orders of magnitude, which means that the controllers are decoupled in time, both controllers still provide the voltage amplitude of the inverter. Overriding the voltage controller thus enhances the stability of the control. The time delay brings two further advantages. Firstly, the voltage controller only restarts for four periods after the fault has been cleared, which means that it only controls the voltage amplitude when u_{PCC} is restored to the normal band. Secondly, in the first milliseconds of the occurrence of the fault, the voltage controller additionally supports the current limiting controller in order to adapt u_{set} more quickly to the fault situation. The voltage regulator is overridden by setting the proportional and the integral part of the regulator to zero. The override is triggered by the fault detection signal. For tests in the laboratory, which only focused on a voltage drop in the amplitude, this method was sufficient as a current limiter. For the tests presented in chapter V on the behaviour in the event of grid faults with the power hardware-in-the-loop system, a correction variable in the phase angle δ_{corr} is also required. The procedure for determining the phase angle correction is shown in Fig. 7.

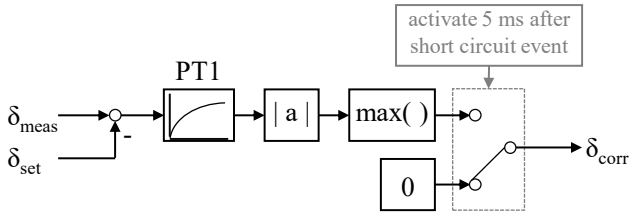

Fig. 7. Block diagram for calculating the correction of the phase angle correction value

The internal reference value of the phase angle is subtracted from the measured phase angle of the voltage. This angle difference is first filtered by a PT1 delay. Then the absolute value is determined and the maximum value is selected over time. In order to avoid a simultaneous reaction with the voltage correction, a delay in the first reaction is implemented. In this case the delay amounts to five ms. This also has the advantage that the adjustment of the phase angle δ_{corr} only reacts when a single reduction of the amplitude u_{corr} after five ms has not caused the current to fall below the maximum current.

IV. Implementation of Current Limitation in Grid Forming Inverters and Laboratory Testing

The current limitation for grid fault situations described in chapter III is integrated into an existing GFI control and implemented on a rapid prototyping inverter. The GFI has a nominal power S_n of 10 kVA and can be operated up to 15 kVA in overload for temporary periods. The functionality will also be tested in the elenia energy labs [15].

A. Structure of the laboratory setup

Component tests are carried out to evaluate the behaviour of the GFI in case of grid fault situations in a 400 V micro grid. The outline of the test setup and different measuring points are depicted in Fig. 8.

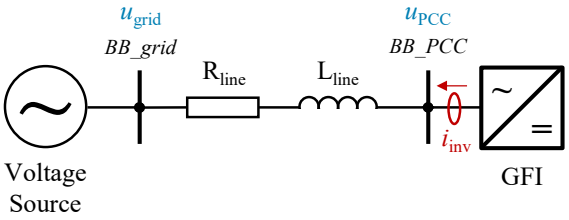

Fig. 8. Laboratory setup for the component tests

The GFI is connected to a busbar *BB_PCC* where the voltage of the inverter $u_{PPC}(t)$ and the injected current $i_{inv}(t)$ are measured. The external grid is represented by an ideal voltage source for conducting grid faults. For this purpose, symmetrical voltage dips will be specified using a 45-kVA inverter as voltage source to emulate three-phase short circuits. The grid voltage $u_{grid}(t)$ is measured at the busbar *BB_grid*. Both busbars are coupled via an impedance to map the lines and transformers of any desired type. For these studies, an ohmic value of $R_{line} = 300$ mΩ and an inductive value of $L_{line} = 0.5$ mH were chosen. The fault clearance is realised by immediately resetting the voltage to its nominal value u_{nom}.

B. Results of the component test

Various voltage dips are specified by reducing the amplitude of the external voltage source. Since the fault situations are only replicated by an amplitude reduction of the voltage source, no correction of the phase angle is required. Therefore, δ_{corr} provides no contribution and is set equal to zero for these studies. The measurements for an amplitude dip to a voltage of $u_{grid} = 0.7$ p.u. at t = 0 s are shown in Fig. 9.

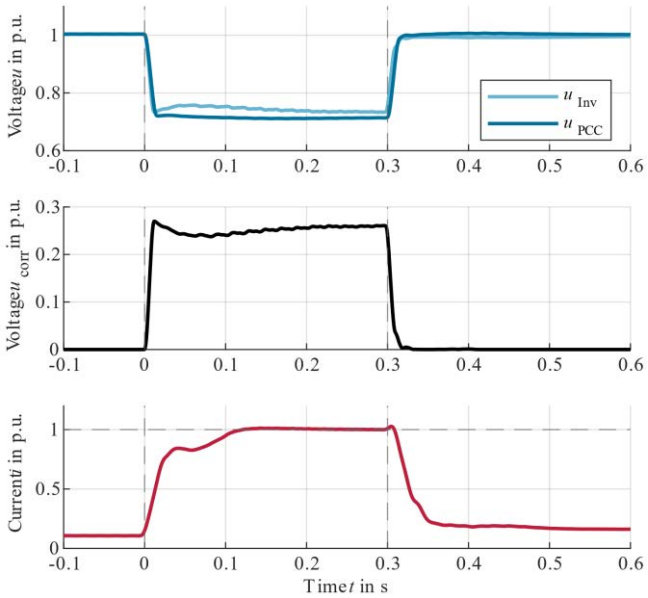

Fig. 9. Measurements and setpoints of the control during fault simulation as amplitude reduction in case of a voltage dip to 0.7 p.u.

The upper plot (blue) shows the voltage which is to be understood as the internal setpoint output voltage u_{inv} of the inverter in front of the filter. In the same plot, the measured output voltage u_{PCC} is also shown, which is present at the point of common coupling. A diagram of the setup was given in Fig. 5 (a). In general, the set voltage follows the external voltage drop to avoid very large over-currents. At the same time the

best possible support for the voltage drop is attempted, while remaining within the technical limits of the maximum possible current. The contribution of current limitation in terms of u_{corr} is shown in the middle part of the diagram (black). Because the current limitation overrides the regular voltage controller, the amplitude value u_{set} is set to 1 p.u and u_{inv} results from $u_{inv} = u_{set} - u_{corr}$. The lower plot of the diagram (red) shows the corresponding inverter current in relation to the nominal current. The current initially reacts slower, which is on the one hand caused by the impedance and mainly by the inductance in the line and on the other hand by the dynamics of the PI controller of the current limitation. After approx. 100 ms the current limitation reaches the maximum contribution in the current from in this case $i = 1.0$ p.u. After 300 ms the grid fault is cleared. The current limitation then slowly reduces the amount of voltage correction u_{corr} to avoid large reactive power peaks in order to avoid stressing the grid. On occurrence of the fault, during the fault and during the fault clearing, the inverter currents that are fed in remain in a sinusoidal shape, as shown in Fig. 10.

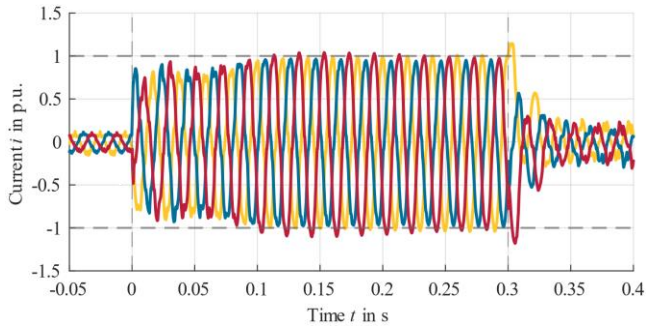

Fig. 10. Plot of the three-phase output currents of the GFI during a short-circuit event with active current limitation

The output current reacts within a few milliseconds and then drives the current to the maximum value via the PI controller. This remains at 1 p.u. for the duration of the short-circuit and the over-current decreases again with a time delay after the fault has been cleared.

C. *Maintenance of the grid forming control in grid fault situations*

The approach used in this thesis to limit the output currents of a GFI was chosen in order not to significantly affect the characteristic control of a GFI, but to maintain the stabilising behaviour during sudden power variations. The following test is supposed to show that the stabilising effect is still functional even in short-circuit situations. For this purpose, during a long short circuit situation period of 2s a frequency jump from 50.0 Hz to 49.8 Hz at $t = 1$s is specified by the voltage source. Synthetic frequency jumps on GFIs in laboratories generally tend to provide significant active power responses and are often used to show the provision of instantaneous power reserve through inertia, see [5] and [6]. The voltage amplitude is reduced to 0.5 p.u. for the fault situation. The pre-fault active power supply of the GFI is $p_{set} = 0.1$ p.u. and no reactive power setpoint q_{set} was specified. Fig. 11 shows in two plots the measured values of the voltage and frequency which have been applied to the test grid as disturbance factors. In further plots the measured current, as well as the active and reactive power are given in p.u.

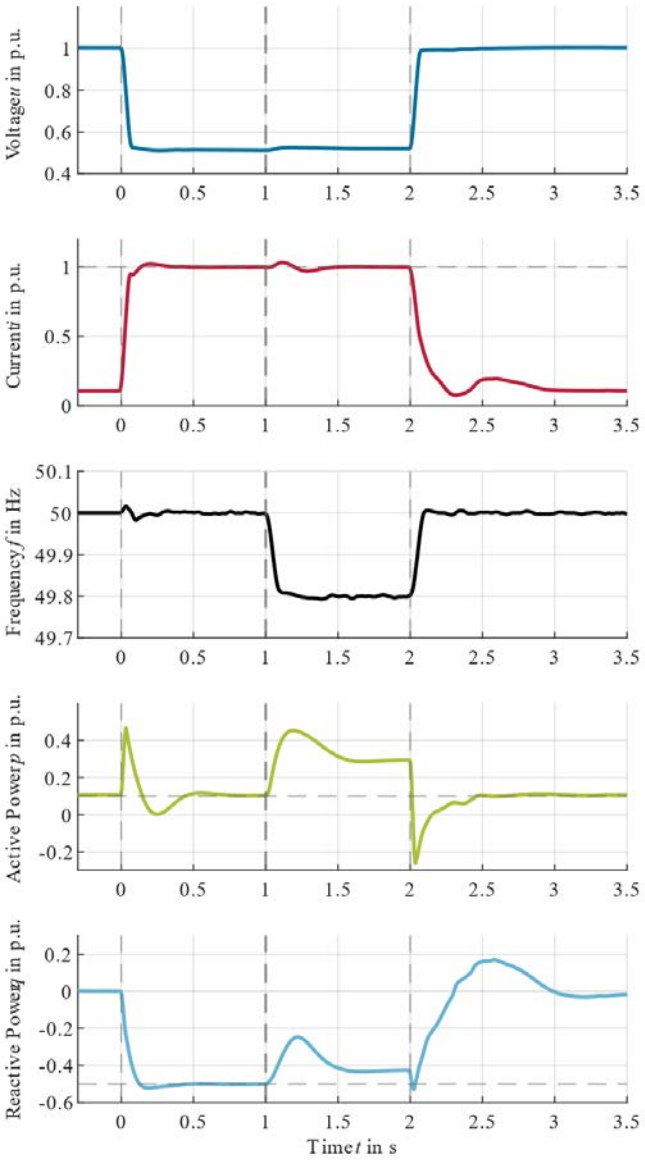

Fig. 11. Instantaneous power adjustment to a frequency step during a symmetrical short circuit event in current limitation mode

In the time range from 0 s to 1 s, the current limitation reacts as in the previous test and attempts to feed in the maximum current to support the grid. Reactions in the active and reactive power are very clear when a fault occurs, but due to the long short-circuit time, they are then returned to their setpoints. The splitting into active and reactive power results from the outer connection and is not controlled directly. At time $t = 1$ s the frequency step is initiated and the GFI reacts with a significant increase in active power. Since the maximum current is already reached in this moment, the active power rate is increased and at the same time the amount of reactive power is reduced. Both the voltage dip and the frequency step are cleared at time $t = 2$ s. The voltage returns quite fast to its pre-fault value, while the fault current from the inverter gradually decreases.

This functional test shows that the stabilising effect of a GFI continues even in short-circuit situations, which is due to the fact that the frequency control of the GFI for current limitation is both activated and remains unchanged. A current

limiting approach that changes to the current-controlled mode would not have this advantageous behaviour.

V. Analysis with a Power Hardware in the Loop System

The preceding component tests for functional testing of the current limitation show that safe grid parallel operation of GFIs in fault situations is possible. In order to carry out further studies, a power hardware-in-the-loop (PHIL) system is used to study the behaviour of the GFI in a power grid during a grid fault. This extension of the test setup also allows for realistic effects, such as the location of the fault, external grids of a higher voltage level, transformers, overhead lines and cables. Furthermore, the three-phase short circuit is no longer simulated by a voltage dip, but is modelled by a low-resistance connection of the three phases and the earth potential. In the following, the technical implementation in the laboratory is presented first.

A. Structure of the power hardware-in-the-loop tests

Here, a real-time simulation is combined with a power amplifier as AC/AC converter. The exchange of setpoint and measurement data is carried out via analogue signals. Fig. 12 describes the basic structure based on the previous set-up of the laboratory in Fig. 8.

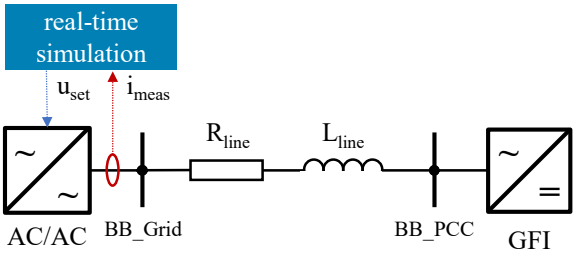

Fig. 12. Laboratory setup for the PHIL tests

PHIL systems combine real-time simulations with hardware components so that the behaviour of existing grid components within a predefined simulated power supply grid can be tested, evaluated and optimised. Both the component's impact on the operation of the supply network and the influence of the grid feedback on the component can be analysed. Using the PHIL system for technical development offers the advantage of flexibility, controllability and realism. Furthermore, the reproducibility of test scenarios and worst-case conditions is given and also investigations under conditions which cannot be created synthetically, e.g. in field tests, are feasible. When working with real-time simulators, it is always important to ensure that new setpoints can be implemented in real time. However, the exact definition of real-time relates then to the individual case of the application. When measuring the closed control loop including measurement data feedback in the PHIL system for this setup, a reaction time of 150 µs was measured. For the observed short-circuit situations, this is sufficiently small in order to qualify as real-time capability.

B. Test grid used for the analysis of short circuit situations

With the use of the PHIL system, it is possible to create short circuit events at different points in the grid and to examine their effects on the current limitation of the GFI. The IEC TR 60909-4 for low voltage benchmark grid offers the advantage of being able to study a short circuit on one of the parallel lines as well as in a single string of the low voltage grid [16]. Fig. 13 shows the test grid and the considered short-circuit points.

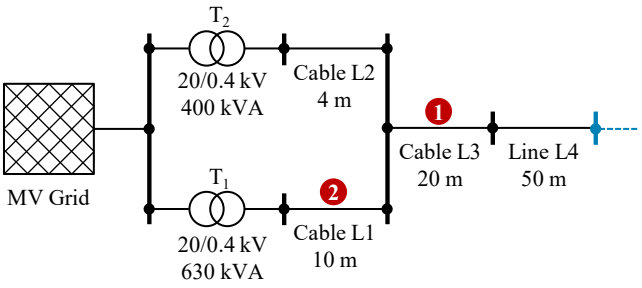

Fig. 13. IEC TR 60909-4 grid for testing FRT behaviour with two different grid fault locations [16]

For this purpose, the point of occurrence of a symmetrical short circuit on a single line 2 and on the busbar of the medium voltage network 3 are considered. As already mentioned, instead of a predefined voltage setpoint change, the switching of a low-resistance resistor is used to imitate the grid fault. With a phase resistance of $R_f = 0.11$ mΩ and a resistance to the earth potential of $R_{fE} = 100$ mΩ, a full three-phase short circuit is emulated.

C. Results of the PHIL studies on the IEC TR 60909-4

In order to show the difference between a modelled fault via a voltage source with amplitude reduction and a simulated fault with a fault impedance, two exemplary tests are presented. In both tests a severe grid fault is simulated so that a voltage dip of $u_{PCC} \approx 0.05$ p.u. is applied at the common coupling point. As opposed to the studies in chapter IV, the current limitation had to be operated with the phase angle correction δ_{corr} to remain stable. At the first test, the fault occurs on cable L3 shown in Fig. 13. The measured voltage in amplitude (blue line) and phase angle ϑ (orange line) and the current *i* in p.u. (red line) are displayed on Fig. 14. The phase angle is shown as a difference to the pre-fault value.

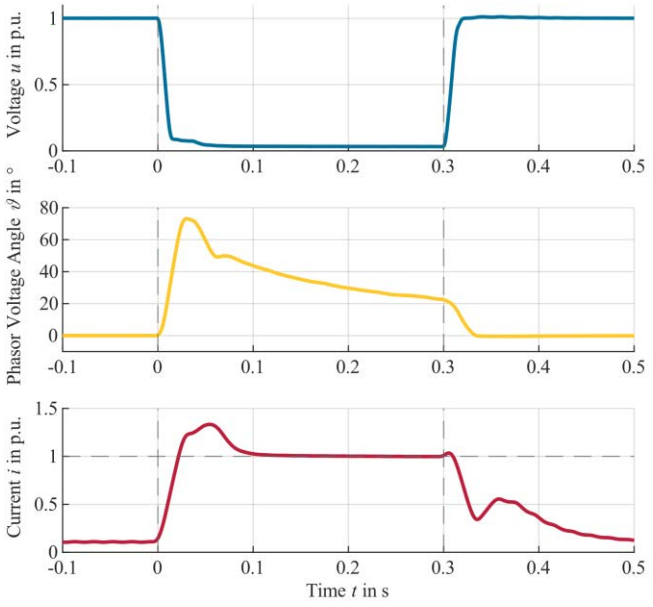

Fig. 14. Measurements of the PHIL tests with simulated grid fault in IEC TR 60909-4 grid and fault location on cable L3

The deep voltage dip to 0.05 p.u. can be handled with the presented approach of current limitation and the inverter remains on the grid. Although there is an overshoot in the current, which reaches approx. 1.3 p.u., this oscillation returns to the maximum value after approx. 100 ms. Especially noticeable in this case is the large phasor voltage angle step ϑ (orange line) that occurs in the event of a grid fault occurrence. Since the phase angles δ are rotating quantities, the angle ϑ is related to a fixed rotating reference system to demonstrate the response during the fault and is determined according to (2).

$$\vartheta = \delta_{PCC} - \delta_{ref} \tag{2}$$

The phasor voltage angle increases by more than 70° at the first moment of the grid fault. This then decreases slightly over the fault duration due to the droop in the normal frequency controller of the GFI. The phase angle deviation also returns to zero with the fault clearance at t = 300 ms.

In a second test, the fault location in the test grid is modified. The other basic conditions remain the same. Also, in this case the measurement results are shown in Fig. 15.

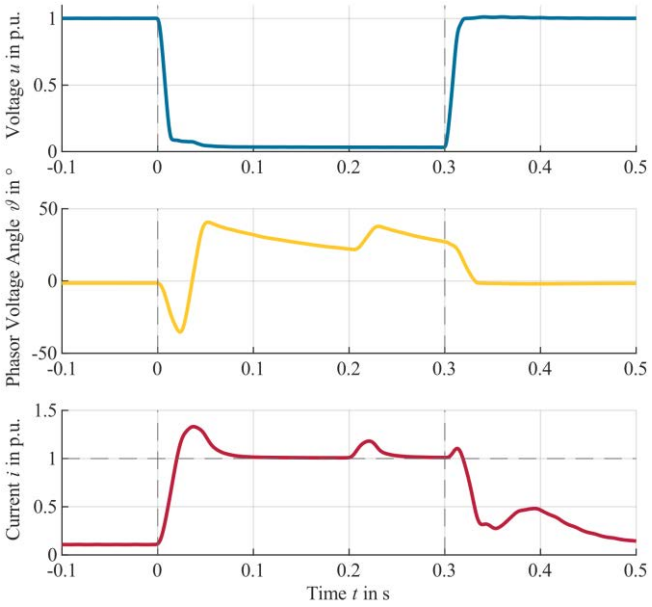

Fig. 15. Measurements of the PHIL tests with simulated grid fault in IEC TR 60909-4 grid and fault location on cable L1

When considering the phasor voltage angle (orange line) in the middle part of Fig. 15, it can be seen that the angle first oscillates when the short circuit occurs. Whether this is caused by the control itself or by the various transient power flows in the IEC 60909 network must be analysed in further studies. The short-term angular reaction after 200 ms is due to an unintended angle adjustment by the control mechanism. Since the frequency controller is not overdriven, the sudden intervention in the phase angle triggers swinging oscillations. This shows that there is still a need for optimisation, especially with such current-limiting control approaches, and that these approaches have to be tested in different grid situations.

VI. Discussion of the Results and Outlook

Current limiting in GFI's synchronous virtual machine control is a necessary behaviour to protect the inverter and to ensure power supply continuity in the event of grid faults. Nevertheless, the dynamic behaviour of the individual inverter always deviates from the model of the synchronous machine and brings its own dynamics into the grid. For this reason, suitable requirements for such current limitations must be coordinated at an early stage, which on the one hand fulfil the function of a current limitation and on the other hand exhibit a defined dynamic behaviour, which can also be considered predictable. In this paper a current limitation control was presented, which can handle the presented situations and laboratory tests and fulfils its own set requirements.

In addition to the requirements, the functions themselves and their optimal integration into existing controls also need to be further examined. In this case, the transition from the regular voltage controller to current limitation is challenging. Currently, the current limitation will be activated if the value falls below 0.85 p.u. When voltage drops in this range, special attention has to be paid to a well-balanced transition between the two states.

The control method presented in this paper for the short-term adjustment of the phase angle has led to a stable and reliable connection of the inverter to the grid. However, inaccurate phase angle increases during the short-circuit were experienced. This could not be solved within the scope of this paper but the knowledge gained from this provides a basis for further research and development work. As the times of the inaccurate phase influence are clearly recognisable in the measurements, however, this does not distort the statements made about the parameters which could in principle be caused by the grid topology.

The tests with the power hardware-in-the-loop system have shown that the single focus on the voltage amplitude is not sufficient for a realistic short circuit case. It has been shown that high swinging oscillations are responsible for this. Consequently, it is also necessary to control the phase angle in short-circuit situations. Therefore, to evaluate the designed current limitation, not only voltage drops but also changes in the phase angle must be investigated. While phase angle steps are not a challenge for normal current-controlled inverters, GFIs in general are very sensitive to phase angle steps. Existing requirements for grid codes focus mainly on the amplitude of the voltage drop [9]. For future considerations regarding GFIs, the phase angle reaction must also be included.

VII. Conclusion

Grid forming inverters with a virtual synchronous machine control necessarily require a current limitation for stable operation on parallel mode connected to the grid in order to be able to react suitably to grid fault situations. The conflict of objectives in this case is to avoid modifying the behaviour of a virtual synchronous machine while maintaining the technical limits of the hardware. For this purpose, a method was presented in this paper. The model is controlled in such a way that the maximum permissible short-circuit current and thus also the maximum short-circuit power is provided. For this purpose, a method for amplitude reduction as well as phase angle correction were designed and integrated into an existing model of a grid forming inverter. A suitable fault detection ensures that the current limitation only has an effect in the defined fault situations. Furthermore, it has been shown it is useful to override the regular voltage regulation in fault situations so that it maintains the pre-fault value. This prevents high compensating currents during fault detection, so that during this time the voltage controller is blocked by the current limiting function. The frequency control in turn remains unchanged to allow instantaneous active power changes.

The presented approach was transferred into a model and its functionality was tested using a rapid prototyping inverter. Considering the typical requirements for fault-ride-through behaviour based on the voltage amplitude, it could be shown in laboratory tests that an exclusive reduction of the voltage amplitude represents a suitable current limitation. Following this, more detailed analyses were carried out using a power hardware-in-the-loop system using the IEC TR 60909 benchmark grid with simulated grid faults. Here it became clear that without a suitable adjustment of the phase angle, no deeper voltage dips could be handled, as this resulted in very large phase angle steps of up to 70° when the grid fault occurred.

In the resulting discussion, clearer and more detailed requirements were required, which have to be met by the test conditions of grid forming inverters. Further research in this area must be carried out to analyse if existing low voltage ride through procedures are still suitable for these test methods.

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